



A TRANSISTOR VIDEO AMPLIFIER FOR RADAR DISPLAY

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I. INTRODUCTION

A video amplifier for use in radar display equipment is described as well as an analysis of the use of transistors in this application. The particular circuit was employed in a small X-band radar set suitable for use in navigation and weather reconnaissance service.

A novel circuit is presented which achieves maximum output video voltage for a given supply voltage. As a result, transistor reliability is enhanced due to the minimum device dissipation experienced in the particular mode of operation. A simplification in the overall display circuitry for the radar results from combining both the range intensifying gate and the range mark pulse signal with the video signal within the amplifier proper.

The typical radar receiver produces an output level of one to two volts. In order to drive the display cathode-ray tube adequately the video level must be increased to approximately forty volts. Thus, the video amplifier should provide a voltage gain of forty while presenting an appropriate load on the second detector within the radar receiver. These requirements are fulfilled in this design with a two-stage amplifier employing Fairchild high-reliability silicon transistors. The input stage uses transistor type 2N915 which has a 40 volt V_{CEO} rating and a typical f_T of 400 mc. The output stage uses transistor type 2N2443 which has a 100 volt V_{CEO} rating and typical f_T of 80 mc.

II. CIRCUIT DESCRIPTION

The video amplifier shown in Figure 1, consists of a common-collector stage driving a common-emitter voltage amplifier. The common-collector stage presents a relatively high impedance load to the second detector while effecting a low output impedance and, thus, a voltage source for driving the common-emitter stage. The Miller capacitance of the voltage amplifier is thus isolated from the second detector where otherwise it would produce bandwidth limiting at the detector load. The use of a voltage source for driving the common-emitter stage results in maximum bandwidth for a given collector load.

The 2N2443 common-emitter stage transistor is biased just at the point of collector current conduction. Thus, the collector voltage can swing from nearly the collector supply voltage, V_{CC} , to the saturated value of collector voltage defined by

$$V_{C(sat)} = \frac{R_E V_{CC}}{R_L + R_E} + \frac{R_L V_{CE(sat)}}{R_L + R_E}$$
$$= \frac{R_8 V_{CC} + R_9 V_{CE(sat)}}{R_8 + R_9} \quad (1)$$

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With small base input voltages the transfer characteristic of the stage is non-linear. However the intensifying gate signal, introduced in the base circuit of the common-collector stage, causes the collector current of the common-emitter transistor to pass through the low current non-linear region very rapidly. The resulting drop in collector voltage produces the intensifying or unblanking signal for driving the cathode of the display cathode-ray tube. The video signal is added to the intensifying signal at the input to the common-collector stage and thus the video portion of the composite signal is amplified in the most linear portion of the common-emitter stage transfer characteristic.

A diode clamp circuit at the input to the common-emitter stage causes the composite signal to drive the base of transistor Q_2 with a unipolar signal in the direction which increases collector current from the near cut-off value.

Proper base bias voltage for the 2N2443 output transistor is obtained by utilizing the voltage drop across a silicon diode. As this voltage closely approaches the base-emitter voltage of the transistor, an operating point is obtained that produces a slight forward bias and thus low quiescent collector current. As the voltage drops across both diodes change in the same manner with temperature change, the bias remains essentially constant.

In the schematic diagram of Figure 1, diode D_3 provides the bias voltage for transistor Q_2 . Resistor R_7 allows sufficient current to flow to allow diode D_3 to be forward biased at all times. The bias voltage is supplied to the base of transistor Q_2 through base resistor R_6 . The use of capacitor C_4 across the bias diode allows relatively large current peaks to flow in the clamping circuit while maintaining the bias voltage constant.

The clamping circuit consists of coupling capacitor C_3 , diode D_2 , and base resistor R_6 . As a result of the voltage drop across D_2 , the base voltage of Q_2 swings negative to zero volts. Thus, D_2 goes into conduction producing the clamping potential on capacitor C_3 during the time between the intensifying gate signals. The positive going intensifying and video signals cause D_2 to go out of conduction and drive Q_2 into high conduction. The low frequency response of the clamping circuit must be sufficient to reduce the droop of the intensifying gate to an acceptable minimum.

The video output amplifier uses a shunt peaked load consisting of inductor L_1 and resistor R_9 for obtaining adequate bandwidth in the collector circuit. The simplicity and effectiveness of the shunt peaking scheme is preferred over other arrangements for this application.

The gain of the stage is controlled by the emitter resistor, R_8 . The signal can be directly coupled

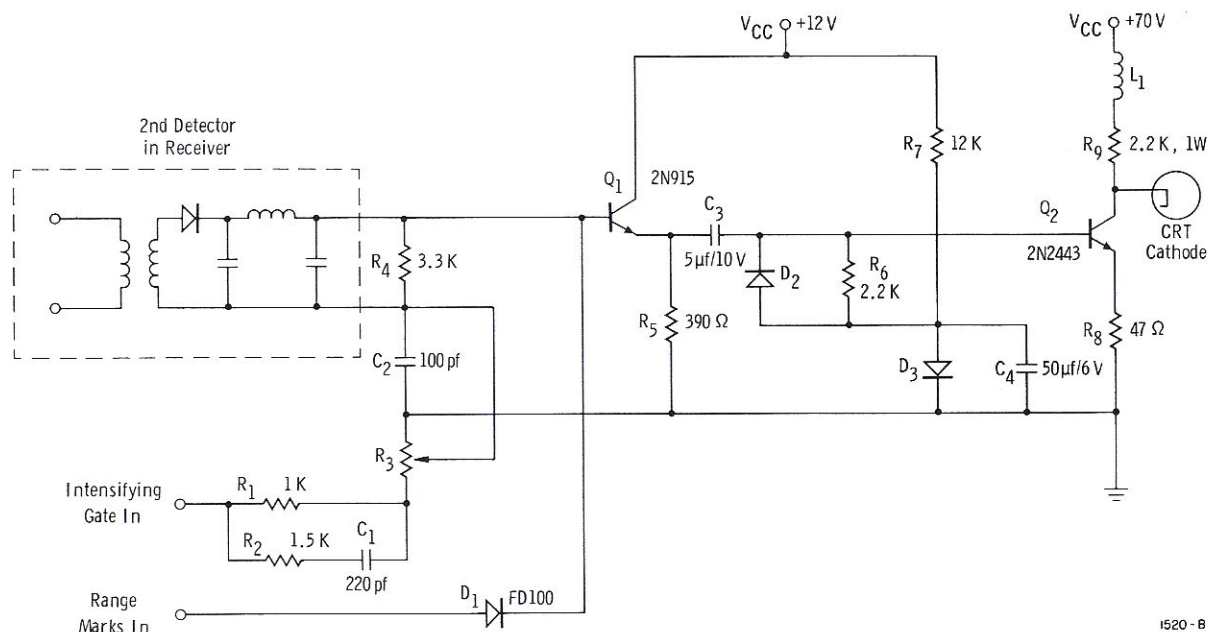


FIG. 1. Schematic diagram of video amplifier.

to the cathode-ray tube since clamping or d-c restoration has effectively retained d-c coupling from the second detector to the amplifier output.

The common-collector stage comprising transistor Q_1 , a 2N915, is similarly out of conduction during the time between intensifying gate signals, being driven on by the gate signal itself. The level of the input gate voltage is controlled by potentiometer R_3 and is normally adjusted to produce a negative going intensifying signal amplitude of 20 volts at the collector of transistor Q_2 . The intensifying gate is coupled in through resistors R_1 and R_2 and capacitor C_1 .

The range marks are coupled into the base of transistor Q_1 through diode D_1 . The second detector diode and diode D_1 form a logical "OR" gate so that either video or range marks are coupled in depending upon which signal has the largest instantaneous amplitude.

Since one of the two diodes will be out of conduction at any one time (except for the very small transient turn off interval), the range mark source and second detector are effectively isolated from each other.

The second detector circuit is by-passed for i-f frequencies by capacitor C_2 . This expedient prevents possible instabilities due to feedback within the i-f amplifier from the second detector. The time constant, consisting of capacitor C_2 and the effective resistance at the tap on resistor R_3 , must be sufficiently small so that the rise time of the intensifying gate is not adversely affected.

III. DESIGN OF COMMON-EMITTER STAGE

The common-emitter video output stage must be capable of supplying a video signal to the display cathode-ray tube of approximately 60 volts peak-to-peak. This signal is composed of 20 volts of unblanking or intensifying voltage and 40 volts of received signal with range marks superimposed. The required value of collector supply voltage V_{CC} is (see Appendix):

$$V_{CC} = \frac{e_{o(max.)} (A_V + 1)}{A_V} + V_{CE(min.)} \quad (2)$$

Substitution of values for the maximum output voltage $e_{o(max.)} = 60$ volts, the voltage gain $A_V = 40$, and the lowest allowable collector to emitter voltage that will prevent saturation, $V_{CE(min.)} = 5$ volts.

$$\begin{aligned} V_{CC} &= \frac{60 (40 + 1)}{40} + 5 \\ &= 66.5 \text{ volts} \end{aligned}$$

A value of $V_{CC} = 70$ volts is thus practical in the actual circuit. The transistor should have an LV_{CEO} rating of approximately 80 volts for use in the circuit. Note that the 2N2443 transistor used is rated at 100 volts, a conservative value for this design.

The video bandwidth of 5 mc in this stage may be readily obtained with silicon-planar transistors. The use of shunt peaking allows a larger value of collector load resistance than could be obtained without peaking for a given bandwidth. This expedient reduces the required collector current and thus device dissipation for a given output voltage. A bandwidth improvement factor of 1.8 can be obtained with the resulting overshoot of only 5%. The collector load resistor, R_L , in Figure 1A can be determined from the uncompensated bandwidth, B_μ , and the total shunt capacitance, C'_T , as follows:

$$B_\mu = \frac{B}{1.8} = \frac{5 \text{ mc}}{1.8} = 2.78 \text{ mc} \quad (3)$$

$$C'_T = C_{oe} + C_{ki} + C$$

$$C'_T = C_{oe} + C_{ki} + C_s$$

$$= 15 + 5 + 5$$

$$= 25 \text{ pf} \quad (4)$$

$$\begin{aligned}
 R_L &= \frac{1}{2\pi B_\mu C_T'} \\
 &= \frac{1}{2\pi(2.78 \times 10^6)(25 \times 10^{-12})} \\
 &= 2290 \Omega
 \end{aligned} \tag{5}$$

A standard value of 2.2K is used in the actual circuit and in computing the peaking coil L_C as follows:

$$L_C = M R_L^2 C_T' \tag{6}$$

For an improvement factor of 1.8, $M = 0.46$ thus solving equation 6.

$$\begin{aligned}
 L_C &= 0.46 (2.2 \times 10^3)^2 (25 \times 10^{-12}) \\
 &= 55.7 \mu h
 \end{aligned}$$

The value of the emitter resistance is calculated to allow the proper stage gain and is given by

$$\begin{aligned}
 R_E &= \frac{R_L}{A_V} \text{ (See Appendix)} \\
 &= \frac{2200}{40} \\
 &= 55 \Omega
 \end{aligned}$$

As shown in the Appendix, the bandwidth limiting factor is primarily the collector load network. The emitter feedback configuration of the common emitter stage results in very large bandwidth of the transadmittance function. Therefore, the transistor has minimal effect on the 5 mc band of interest.

Dissipation in the common-emitter transistor depends upon the content of the received signal. However, maximum dissipation occurs when $i_c = V_{CC} / [2(R_L + R_E)]$ and represents the worst condition of signal content from the standpoint of device heating. The dissipation under this condition is

$$\begin{aligned}
 P_{d(max.)} &= \frac{V_{CC}^2 A_V}{4R_L (A_V + 1)} \\
 &= \frac{(70)^2 (40)}{4(2.2 \times 10^3) (40 + 1)} \\
 &= 0.541 \text{ watts}
 \end{aligned} \tag{7}$$

The maximum dissipation in the actual circuit is obtained by multiplying the maximum dissipation by the effective duty cycle which itself is maximum on the longest radar range.

$$P'_{d(max.)} = P_{d(max.)} (\text{Range})(\mu\text{sec}/\text{mile})(\text{PRF}) \tag{8}$$

For the particular radar in which the amplifier was used having a maximum range of 25 miles, and a pulse recurrence frequency (PRF) of 930 pulses per second, the maximum device dissipation $P'_{d(max.)}$ is as follows

$$\begin{aligned}
 P'_{d(max.)} &= (.541) (25) (10.76 \times 10^{-6}) (930) \\
 &= 0.135 \text{ watts}
 \end{aligned}$$

Thus, the dissipation is safely within the 0.8 W free air rating of the Fairchild 2N2443.

The maximum average collector current required from the power supply is

$$\begin{aligned}
 i_{c(max.)} &= \frac{V_{CC} (\text{Range}) (10.76 \times 10^{-6}) (\text{PRF})}{2(R_L + R_E)} \\
 &= \frac{(70) (25) (10.76 \times 10^{-6}) (930)}{2(2200 + 55)} \\
 &= 3.84 \text{ ma}
 \end{aligned} \tag{9}$$

IV. DESIGN OF COMMON-COLLECTOR STAGE

The low impedance source for driving both the diode clamp circuit and the common-emitter stage can be obtained readily from the common-collector stage. The output resistance of the stage is determined as follows:

$$R_o \approx \frac{R_E \left[R_q / \beta_o + 1 \right]}{R_E + R_q / (\beta_o + 1)} \quad (10)$$

A value of second detector output resistance R_q is assumed to be 2.2K ohms. A suitable value for $\beta_o = 40$. The value of R_E may be determined by allowing a value of collector current to flow such that β_o is maximum while the emitter voltage is at its average value during the intensifying period. Thus, the value of

$R_E = \frac{1 \text{ volt}}{5 \text{ mA}} = 200 \Omega$, and a practical value of 220 Ω is used in the circuit and solving equation 10 yields

$$R_o \approx \frac{220 \cdot 2.2 \times 10^3 / (40 + 1)}{220 + 2.2 \times 10^3 / (40 + 1)}$$

$$\approx 43.1 \Omega$$

The average current i_{c1} required by the common-collector stage is as follows:

$$\begin{aligned} i_{c1} &= i_c \times \text{Range (Miles)} \times \mu\text{sec/mile} \times \text{PRF} \\ &= (5 \times 10^{-3}) (25) (10.76 \times 10^{-6}) (930) \\ &= 1.25 \text{ mA} \end{aligned} \quad (11)$$

The maximum dissipation of the common-collector stage is therefore

$$\begin{aligned} P_{d(\max.)}'' &= \left[V_{CC} - E_{e(\text{Ave})} \right] i_{c1} \\ &= (12 - 1) (1.25 \times 10^{-3}) \\ &= 13.75 \text{ mW} \end{aligned} \quad (12)$$

The input capacitance C_{IN} of the common-emitter stage is primarily Miller capacitance and is given as follows:

$$\begin{aligned} C_{IN} &= C_s + C_{ob} (A_V + 1) \\ &= 6 + 5 (40 + 1) \\ &= 211 \text{ pf} \end{aligned} \quad (13)$$

The RC limited bandwidth at the emitter of the common-collector stage is

$$\begin{aligned} B_\mu &= \frac{1}{2\pi R_o C_{IN}} \\ &= 2\pi (43.1) (211 \times 10^{-12}) \\ B_\mu &= 17.5 \text{ mc} \end{aligned} \quad (14)$$

The bandwidth of the common-collector stage is considerably higher than that of the common-emitter stage so that bandwidth shrinking from the cascaded stages is minimal. Similarly, the second detector bandwidth is sufficiently larger than the required bandwidth of 5 mc, also for the purpose of reducing bandwidth shrinking.

V. CONCLUSION

The use of two silicon planar transistors adequately satisfies the requirement for a wide-band video amplifier suitable for use in radar display equipment. A convenient means is also provided for combining both the intensifying gate and the range marks with the video information. The mode of operation allows minimum dissipation in the transistors resulting in low power drain as well as increased reliability.

APPENDIX

1. Analysis of common-emitter stage

The common-emitter stage operating with a minimal quiescent collector current provides the maximum excursion of collector voltage. The required collector supply voltage for this mode of operation may be determined by first defining the maximum collector current that is permitted to flow with maximum signal input to the circuit

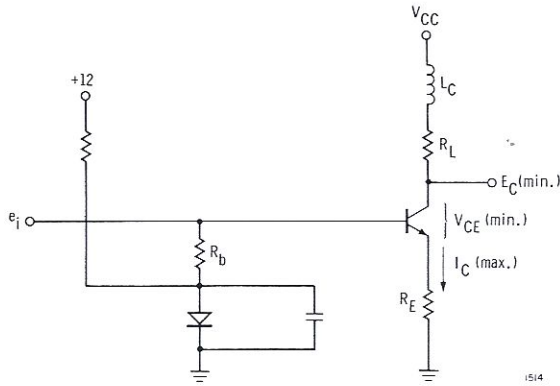


FIG. 1A. Schematic of common-emitter stage (voltage amplifier)

in Figure 1A. The maximum collector current $I_{C(max.)}$ is as follows:

$$I_{C(max.)} = \frac{V_{CC} - V_{CE(min.)}}{R_L + R_E}$$

where $R_E = \frac{R_L}{A_V}$

$$\begin{aligned} I_{C(max.)} &= \frac{V_{CC} - V_{CE(min.)}}{R_L + R_L/A_V} \\ &= \frac{A_V [V_{CC} - V_{CE(min.)}]}{R_L (A_V + 1)} \end{aligned} \quad (1A)$$

The lowest collector voltage normally attained is

$$E_{C(min.)} = V_{CC} - e_{o(max.)}$$

The collector supply voltage V_{CC} is

$$\begin{aligned} V_{CC} &= E_{C(min.)} + R_L I_{C(max.)} \\ &= V_{CC} - e_{o(max.)} \\ &\quad + \frac{R_L A_V [V_{CC} - V_{CE(min.)}]}{R_L (A_V + 1)} \\ &= \frac{e_{o(max.)} (A_V + 1)}{A_V} + V_{CE(min.)} \end{aligned} \quad (2A)$$

The dissipation in the common-emitter transistor is shown below:

$$P_d = V_{CC} i_c - i_c^2 (R_L + R_E) \quad (3A)$$

Maximum dissipation occurs when

$$\frac{dP_d}{di_c} = 0, \quad \frac{dP_d}{di_c} = V_{CC} - 2i_c (R_L + R_E),$$

$$V_{CC} - 2i_c (R_L + R_E) = 0,$$

$$\text{and } i_c = \frac{V_{CC}}{2(R_L + R_E)};$$

then solving equation (3A)

$$\begin{aligned} P_{d(max.)} &= V_{CC} \left[\frac{V_{CC}}{2(R_L + R_E)} \right] - \left[\frac{V_{CC}}{2(R_L + R_E)} \right]^2 (R_L + R_E) \\ &= \frac{V_{CC}^2}{2(R_L + R_E)} - \frac{V_{CC}^2}{4(R_L + R_E)} \\ &= \frac{V_{CC}^2}{4(R_L + R_E)} \end{aligned}$$

The emitter resistance R_E may be equated to R_L/A_V so that,

$$P_{d(max.)} = \frac{V_{CC}^2}{4(R_L + R_L/A_V)}$$

$$P_{d(max.)} = \frac{V_{CC}^2 A_V}{4R_L (A_V + 1)} \quad (4A)$$

2. Voltage gain equations

Using the approximate equivalent circuit of the video transistor, the overall equivalent circuit of the common-emitter stage is shown in Figure 2A. The collector-base capacitance C_C is shown as a Miller capacitance shunting the emitter diffusion capacitance. The input impedance, h'_{ie} , to the amplifier at terminals b - g is given in the expression

$$h'_{ie} = r'_b + \frac{R}{1 + s C_T R} + R_E (h_{fe} + 1)$$

where

$$C_T = 1/(\omega_\beta R) + C_C (A + 1)$$

$$= \left[1 + \omega_\beta R C_C (A + 1) \right] / (\omega_\beta R)$$

$$h_{fe} = (\omega_\beta \beta_o) / (\omega_\beta + s)$$

$$s = \sigma + j\omega$$

so that the equation for h'_{ie} becomes

$$h'_{ie} = r'_b + \frac{R}{1 + sR \left[\frac{1 + \omega_\beta R C_C (A + 1)}{\omega_\beta R} \right]}$$

$$+ R_E \left(\frac{\omega_\beta \beta_o}{\omega_\beta + s} + 1 \right)$$

$$= r'_b + R_E + \frac{\omega_\beta \beta_o R_E}{\omega_\beta + s}$$

$$+ \frac{\omega_\beta R}{\omega_\beta + s \left[1 + \omega_\beta R C_C (A + 1) \right]} \quad (5A)$$

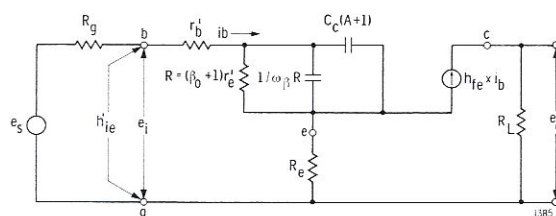


FIG. 2A. Equivalent circuit of emitter-feedback stage.

The gain of the amplifier can be expressed as follows:

$$A_V = e_o / e_i$$

$$= -(h_{fe} i_b R_L) / (i_b h'_{ie}) = -(h_{fe} R_L) / h'_{ie}$$

Substituting the equations for h'_{ie} and h_{fe} in the above and simplifying yields the following:

$$A_V = -(\omega_\beta \beta_o R_L) / \left\{ \omega_\beta \left[R_E (\beta_o + 1) + r'_b \right] \right.$$

$$\left. + s(R_E + r'_b) + \frac{\omega_\beta R (\omega_\beta + s)}{\omega_\beta + s \left[1 + \omega_\beta R C_C (A_V + 1) \right]} \right\} \quad (6A)$$

The third term in the denominator still contains an A_V term. The final solution for A_V in the above equation involves a lengthy quadratic that may be simplified as follows by taking the limit as s approaches 0.

$$\lim_{s \rightarrow 0} \frac{\omega_\beta R (\omega_\beta + s)}{\omega_\beta + s \left[1 + \omega_\beta R C_C (A_V + 1) \right]} = \omega_\beta R$$

Thus the expression for low frequency gain becomes

$$A_{V_o} = - \frac{\omega_\beta \beta_o R_L}{\omega_\beta \left[R_E (\beta_o + 1) + r'_b \right] + \omega_\beta R}$$

$$= - \frac{\beta_o R_L}{R_E (\beta_o + 1) + r'_b + R}$$

NOTE: The derivation of the voltage gain and bandwidth equations were extracted from Fairchild APP-67 and reprinted here with modifications for the sake of completeness.

Substituting

$$\begin{aligned}
 R &= (\beta_o + 1) r'_e \\
 A_{V_o} &= - \frac{\beta_o R_L}{R_E (\beta_o + 1) + r'_b + (\beta_o + 1) r'_e} \\
 &= - \frac{\beta_o R_L}{(R_E + r'_e) (\beta_o + 1) + r'_b} \quad (7A)
 \end{aligned}$$

Since

$$(R_E + r'_e) (\beta_o + 1) \gg r'_b \text{ and } (\beta_o + 1) \simeq \beta_o$$

then

$$\begin{aligned}
 A_{V_o} &\simeq - \frac{R_L}{R_E + r'_e} \\
 &\simeq - \frac{R_L}{R_E + 26/I_E} \quad (8A)
 \end{aligned}$$

For the practical video amplifier supplying a high output voltage, the emitter current must be correspondingly high, therefore $r'_e = 26/I_E$ will be small compared to R_E . A further simplification results for A_{V_o} .

$$A_{V_o} \simeq - \frac{R_L}{R_E} \quad (9A)$$

The effect of the third term in the denominator, equation (6A), on the overall gain function is as follows: as $s \rightarrow \infty$ the resulting indeterminate form may be deleted and a determinate form obtained by noting that the

$$\begin{aligned}
 \lim_{s \rightarrow \infty} \frac{f(s)}{F(s)} &= \lim_{s \rightarrow \infty} \frac{f'(s)}{F'(s)} \\
 \lim_{s \rightarrow \infty} \frac{\omega_\beta R (\omega_\beta + s)}{\omega_\beta + s \left[1 + \omega_\beta R C_C (A_V + 1) \right]} &= \frac{R \omega_\beta}{1 + \omega_\beta R C_C (A_V + 1)}
 \end{aligned}$$

The denominator of the limit can be evaluated for a typical video amplifier transistor using the following values:

$$\omega_\beta = \frac{2\pi \times 150 \times 10^6}{\beta_o + 1}; R = (\beta_o + 1) (1\Omega); C_C = 10 \text{ pf};$$

$$A_V = 15$$

$$\begin{aligned}
 \text{Denominator} &= 1 + \left[\frac{2\pi (150 \times 10^6)}{\beta_o + 1} \right] \left[\beta_o + 1 \right] \left[10^{-11} \right] \\
 &\cdot \left[15 + 1 \right] = 1.15
 \end{aligned}$$

The practical limit for the third term in the denominator of the gain function, equation (6A), using typical transistor values is

$$\begin{aligned}
 \lim_{s \rightarrow \infty} \frac{\omega_\beta R (\omega_\beta + s)}{\omega_\beta + s \left[1 + \omega_\beta R C_C (A_V + 1) \right]} &= \frac{R \omega_\beta}{1.15} \\
 \frac{R \omega_\beta}{1.15} &= \frac{(\beta_o + 1) r'_e \omega_\beta}{1.15} \quad (10A)
 \end{aligned}$$

By combining the above term, $\lim D_3$, with the first term, D_1 , in the denominator of A_V , equation (6A), is

$$D_1 + \lim D_3$$

$$\begin{aligned}
 &= \omega_\beta \left[R_E (\beta_o + 1) + r'_b \right] + \frac{\omega_\beta (\beta_o + 1) r'_e}{1.15} \\
 &= \omega_\beta \left[\left(R_E + \frac{r'_e}{1.15} \right) (\beta_o + 1) + r'_b \right]
 \end{aligned}$$

It can be seen that where $R_E \gg r'_e/1.15$, the effect of Miller capacitance has a minimal effect on the denominator of the gain function, therefore, the equation for the gain function becomes

$$A_V = - \frac{\omega_\beta \beta_o R_L}{\omega_\beta \left[R_E (\beta_o + 1) + r'_b \right] + s (R_E + r'_b)} \quad (10.1A)$$

From equation (10.1A), the pole of the gain function is located at (See fig. 3A)

$$s = -\frac{1}{R C'_{be}} \left[\frac{R_E (\beta_o + 1) + r'_b}{R_E + r'_b} \right]$$

If the gain function in Eq. (10.1A) is modified to include the capacitance C'_T normally present in the actual circuit shunting the collector load resistance, R_L , the following results

$$s = -\frac{1}{R C'_{be}} \left[\frac{R_E (\beta_o + 1) + r'_b}{R_E + r'_b} \right]$$

$$s = \frac{1}{R_L C'_T} \left(\frac{1}{2m} \right) (-1 \pm j\sqrt{4m - 1})$$

From equation (10.5A) the zero of the gain function is located at (See Figs. 5A and 6A)

$$A_V = -\frac{\omega_\beta \beta_o R_L}{(1 + s C'_T R_L) \left\{ \omega_\beta [R_E (\beta_o + 1) + r'_b] + s(R_E + r'_b) \right\}} \quad (10.2A)$$

From equation (10.2A), the poles of the gain function are located at (See fig. 4A)

$$s = -\left[\frac{1}{R C'_{be}} \right] \left[\frac{R_E (\beta_o + 1) + r'_b}{R_E + r'_b} \right]; s = -\frac{1}{R_L C'_T}$$

The use of a shunt peaking coil, L_C , for bandwidth compensation modifies the gain function to the following equation:

$$s = -\frac{1}{m R_L C'_T}$$

From the complex frequency plot of equation (10.1A) it is shown that the bandwidth is very wide for the amplifier gain function where the value of R_E is significantly large. The plot also represents the amplifier transadmittance so that the emitter

$$A_V = -\frac{\omega_\beta \beta_o (R_L + s L_C)}{(s^2 L_C C'_T + s R_L C'_T + 1) \left\{ \omega_\beta [R_E (\beta_o + 1) + r'_b] + s(R_E + r'_b) \right\}} \quad (10.3A)$$

The value of the peaking coil is dependent on the rise time improvement or bandwidth compensation desired consistent with the permissible overshoot and is expressed in terms of a parameter m such that

$$L_C = m R_L^2 C'_T \quad (10.4A)$$

Substitution of equation (10.4A) in equation (10.3A) yields the following:

circuit response of the amplifier is simultaneously defined (approximately). Thus, in equation (10) where output resistance is defined in terms of β_o rather than h_{fe} , the simplified equation is valid.

The effect of shunt capacitance across the collector load resistance introduces a second pole on the σ axis. This causes the bandwidth of the practical video amplifier to be significantly reduced over that obtained with the emitter degenerated transistor with a theoretically pure resistive load.

$$A_V = -\frac{\omega_\beta \beta_o (R_L + s m R_L^2 C'_T)}{(s^2 m R_L^2 C'^2_T + s R_L C'_T + 1) \left\{ \omega_\beta [R_E (\beta_o + 1) + r'_b] + s(R_E + r'_b) \right\}} \quad (10.5A)$$

From equation (10.5A) the poles of the gain function are located at (See Figs. 5A and 6A)

The use of shunt peaking allows a bandwidth improvement over that obtained by the $R_L C_T'$ limited case in equation (10.2A). As the parameter m , and thus the value of the peaking inductance, is increased from zero, a single real pole starts from $-1/(R_L C_T')$ and moves toward $-2/(R_L C_T')$ while a second real pole moves from $-\infty$ and coincides with the first real pole at $-2/(R_L C_T')$ when $m = 0.25$. As m is increased further, both poles become complex and follow a circular path approaching the origin at $m = \infty$ as shown in Figure 6A. For values of m up to 0.25, the resulting time response contains no overshoot, because the poles remain on the real axis and can contribute only to neper frequencies rather than radian frequencies. As m is increased beyond 0.25 the time response will contain overshoot due to the radian frequency enhancement by the resulting complex poles. A practical value for $m = 0.46$ is satisfactory for television video amplifiers where the time response overshoot is only 5% for a bandwidth improvement factor of 1.8.

Bandwidth limiting in the amplifier due to the frequency-sensitive elements within the transistor and excluding the effect of the collector-circuit time constant existing in the practical circuit can be expressed by equation (11A) below. The generator resistance, R_S , is included although the Miller effect capacitance is excluded based on the foregoing description.

$$\begin{aligned} \frac{e_o}{e_s} &= - \frac{h_{fe} R_L}{R_S + h'_{ie}} \\ &= - \left(\frac{\omega_\beta \beta_o}{\omega_\beta + s} \right) R_L / \left\{ R_S + r'_b + \frac{R}{1 + sR \left[(1/\omega_\beta R) \right]} \right. \\ &\quad \left. + R_E \left[\frac{\omega_\beta \beta_o}{\omega_\beta + s} + 1 \right] \right\} \\ &= - (\omega_\beta \beta_o R_L) / \left\{ \omega_\beta \left[R_S + r'_b + R + R_E (\beta_o + 1) \right] \right. \\ &\quad \left. + s(R_S + r'_b + R_E) \right\} \quad (11A) \end{aligned}$$

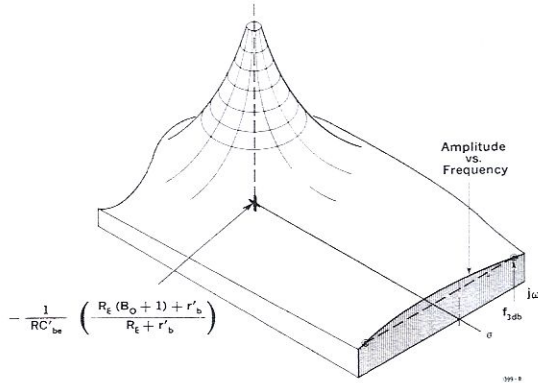


FIG. 3A. Complex frequency plot of amplifier gain function with resistive load (Eq. 10.1A).

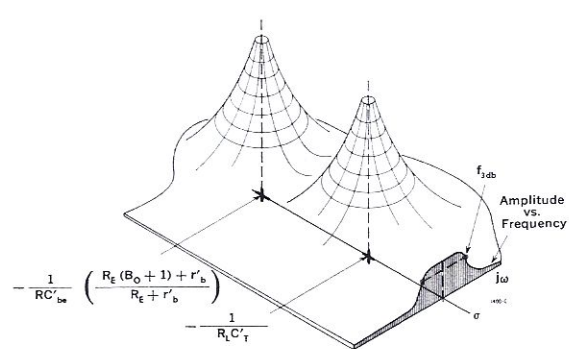


FIG. 4A. Complex frequency plot of amplifier gain function with resistive load shunted by circuit capacitance (Eq. 10.2A).

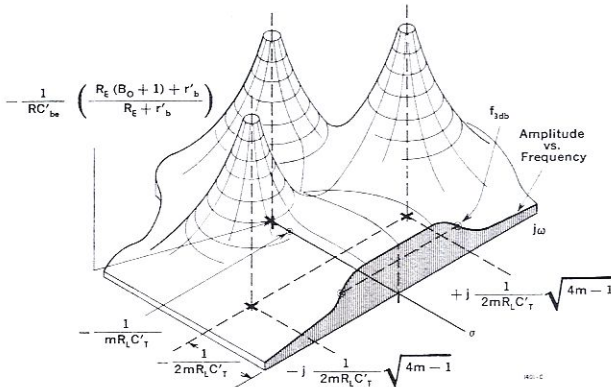


FIG. 5A. Complex frequency plot of amplifier gain function with load consisting of R_L , C_T' , L_C (Eq. 10.3A).

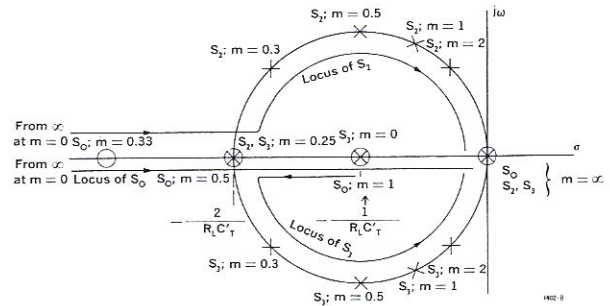


FIG. 6A. Pole-zero locus plot as a function of parameter m .

The 3 db bandwidth occurs at a frequency where the real and imaginary parts of the denominator are equal, which is

$$\begin{aligned}
 & \left| \omega_{\beta} \left[R_S + r'_b + R + R_E (\beta_o + 1) \right] \right| \\
 & = \left| s(R_S + r'_b + R_E) \right| \\
 & \omega_{\beta} \left[R_S + r'_b + R + R_E (\beta_o + 1) \right] \\
 & = \omega_{3db} (R_S + r'_b + R_E) \\
 & \omega_{3db} = \frac{\omega_{\beta} \left[R_S + r'_b + R + R_E (\beta_o + 1) \right]}{R_S + r'_b + R_E} \\
 & f_{3db} = \frac{\frac{f_t}{\beta_o + 1} \left[R_S + r'_b + r'_e (\beta_o + 1) + R_E (\beta_o + 1) \right]}{R_S + r'_b + R_E} \\
 & = \frac{f_t \left[R_E + r'_e + \frac{R_S + r'_b}{\beta_o + 1} \right]}{R_S + r'_b + R_E} \quad (12A)
 \end{aligned}$$

The typical video amplifier transistor and video driver exhibit the following values:

$$\begin{aligned}
 r'_b &= 10 \Omega & R_S &= 45 \Omega \\
 r'_e &= 2 \Omega \text{ at } 13 \text{ mA} & \beta_o &= 40 \\
 R_E &= 56 \Omega & f_t &= 150 \text{ mc} \\
 f_{3db} &= \frac{150 \times 10^6 \left[56 + 2 + \frac{45 + 10}{40 + 1} \right]}{45 + 10 + 56} = 80 \text{ mc}
 \end{aligned}$$

Thus it may be seen that the transistor with emitter feedback has a little effect on the frequency response within the 5 mc band of interest.

3. Analysis of common collector video driver

The equivalent circuit of the video driver is shown in Figure 7A. Collector capacitance C_C will not be taken into account since its effect is much less in the common collector stage than in the emitter feedback amplifier where it was inconsequential.

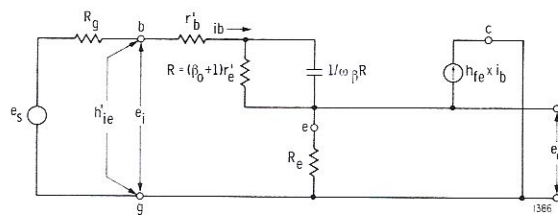


FIG. 7A. Equivalent circuit of common-collector stage.

The input impedance h'_{ie} at terminals b - g is given in the expression below.

$$\begin{aligned}
 h'_{ie} &= r'_b + \frac{R}{1 + s C_{be} R} + R_E (h_{fe} + 1) \\
 &= r'_b + R_E + \frac{R}{1 + \frac{s}{\omega_{\beta}}} + R_E \left(\frac{\omega_{\beta} \beta_o}{\omega_{\beta} + s} \right) \\
 h'_{ie} &= r'_b + R_E + \frac{R \omega_{\beta}}{\omega_{\beta} + s} + \frac{R_E \omega_{\beta} \beta_o}{\omega_{\beta} + s} \quad (13A)
 \end{aligned}$$

The gain of the video driver can be expressed as follows:

$$\begin{aligned}
 A_V &= \frac{e_o}{e_i} = \frac{R_E (h_{fe} i_b + i_b)}{i_b (h'_{ie})} \\
 &= \frac{R_E (h_{fe} + 1)}{h'_{ie}} \\
 &= \frac{R_E \left[\frac{\omega_{\beta} \beta_o}{\omega_{\beta} + s} + 1 \right]}{r'_b + R_E + \frac{R \omega_{\beta}}{\omega_{\beta} + s} + \frac{R_E \omega_{\beta} \beta_o}{\omega_{\beta} + s}} \quad (14A)
 \end{aligned}$$

The expression for low frequency gain A_{V_O} is

$$\begin{aligned}
 A_{V_O} &= \frac{R_E \left[\omega_{\beta} (\beta_o + 1) \right]}{\omega_{\beta} \left[R_E (\beta_o + 1) + R + r'_b \right]} \\
 &= \frac{R_E (\beta_o + 1)}{R_E (\beta_o + 1) + R + r'_b} \quad (15A)
 \end{aligned}$$

In order to derive the bandwidth of the video driver it is necessary to include the effect of its driving source resistance in the voltage gain equation.

$$\begin{aligned}
\frac{e_o}{e_s} &= \frac{R_E(h_{fe} i_b + i_b)}{i_b(h'_{ie} + R_S)} \\
&= \frac{R_E(h_{fe} + 1)}{h'_{ie} + R_S} \\
&= \frac{R_E \left[\frac{\omega_\beta \beta_o}{\omega_\beta + s} + 1 \right]}{r'_b + R_E + \frac{R\omega_\beta}{\omega_\beta + s} + \frac{R_E \omega_\beta \beta_o}{\omega_\beta + s} + R_S} \\
&= \frac{R_E [\omega_\beta (\beta_o + 1) + s]}{\omega_\beta [R_E (\beta_o + 1) + R_S + R + r'_b] + s(R_E + R_S + r'_b)}
\end{aligned}$$

The 3 db bandwidth occurs at a frequency where the real and imaginary parts of the e_o/e_s denominator are equal

$$\begin{aligned}
\left| \omega_\beta [R_E (\beta_o + 1) + R_S + R + r'_b] \right| &= \left| s(R_E + R_S + r'_b) \right| \\
\omega_\beta [R_E (\beta_o + 1) + R_S + R + r'_b] &= \omega_{3db} (R_E + R_S + r'_b) \\
\omega_{3db} &= \frac{\omega_\beta [R_E (\beta_o + 1) + R_S + R + r'_b]}{R_E + R_S + r'_b} \\
f_{3db} &= \frac{\frac{f_t}{\beta_o + 1} [R_E (\beta_o + 1) + R_S + r'_e (\beta_o + 1) + r'_b]}{R_E + R_S + r'_b} \\
&= f_t \frac{\left[\frac{R_S + r'_b}{\beta_o + 1} \right]}{R_E + R_S + r'_b} \quad (16A)
\end{aligned}$$

Typical values for the video driver circuit and the detector source resistance can now be substituted into equation (16A), these are: $R_E = 220 \Omega$, $R_S = 2200 \Omega$, $r'_e = 26/5 \text{ mA} = 5.2 \Omega$, $\beta_o = 40$, $r'_b = 15 \Omega$, and $f_t = 250 \times 10^6$.

Solving for bandwidth

$$\begin{aligned}
f_{3db} &= \frac{250 \times 10^6 \left[220 + 5.2 + \frac{2200 + 15}{40 + 1} \right]}{220 + 2200 + 15} \\
&= 28.6 \text{ mc}
\end{aligned}$$

Thus it can be seen that even with the large value of detector source resistance, the frequency response of the video driver has a small effect on the 5 mc video passband.

LIST OF SYMBOLS

A_V	Voltage gain of stage
B_μ	Uncompensated bandwidth
β_o	Low frequency transistor forward current transfer ratio
C_{oe}	Output capacitance, common-emitter
C_{ki}	CRT cathode input capacitance
C_S	Stray capacitance
C'_T	Total shunt capacitance
L_C	Peaking coil inductance in collector circuit
M	Parameter of peaking coil inductance
$P'_{d(max.)}$	Maximum power dissipation corrected for duty cycle of the common-emitter stage
$P_{d(max.)}$	Maximum power dissipation
$P''_{d(max.)}$	Maximum dissipation of the common-collector stage
R_E	Emitter resistor
R_L	Video load resistance
R_q	Second detector output resistance

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NOTE This application note is one of a series describing a small X-band radar set suitable for use in navigation and weather reconnaissance service which was constructed in the Fairchild Semiconductor Applications Laboratory. The individual sections of this equipment are described in APP-76 through APP-81. (These notes will be distributed as they become available.)